IN THE CLAIMS:

We claim:

1. A memory system comprising a plurality of T-RAM cells arranged in an array, wherein each of the plurality of T-RAM cells includes a thyristor region beneath at least a portion of a transfer gate region.

2. The memory system according to Claim 1, wherein the thyristor region includes a buried vertical thyristor and the transfer gate region includes a horizontally stacked pseudo-TFT transfer gate.

3. The memory system according to Claim 1, wherein each of the plurality of T-RAM cells has a size of less than or equal to $8F^2$.

4. The memory system according to Claim 1, wherein the plurality of T-RAM cells are fabricated on a semiconductor SOI or bulk wafer.

5. The memory system according to Claim 1, wherein a base of the thyristor region is surrounded by a vertical surrounded gate.

6. The memory system according to Claim 5, wherein the vertical surrounded gate contacts a wordline.

7. The memory system according to Claim 1, wherein the thyristor region and the transfer gate region are connected by a lateral epitaxial grown n+ region.

8. The memory system according to Claim 2, wherein a bitline contacts a junction of the stacked pseudo-TFT transfer gate.

9. The memory system according to Claim 2, wherein the stacked pseudo-TFT transfer gate contacts a wordline.

10. The memory system according to Claim 1, wherein each of the plurality of T-RAM cells includes structure for the traversal of at least two wordlines there through.

11. The memory system according to Claim 2, wherein a vertical surrounded gate is aligned with a base region of the buried vertical thyristor.

12. A T-RAM array comprising:

a plurality of T-RAM cells, wherein each of the plurality of T-RAM cells includes a thyristor region beneath at least a portion of a transfer gate region.

13. The array according to Claim 12, wherein the thyristor region includes a buried vertical thyristor and the transfer gate region includes a horizontally stacked pseudo-TFT transfer gate.

14. The array according to Claim 12, wherein each of the plurality of T-RAM cells has a size of less than or equal to $8F^2$.

15. The array according to Claim 12, wherein the plurality of T-RAM cells are fabricated on a semiconductor SOI or bulk wafer.

16. The array according to Claim 12, wherein a base of the thyristor region is surrounded by a surrounded gate.

17. The array according to Claim 12, wherein each of the plurality of T-RAM cells includes structure for the traversal of at least two wordlines there through.

18. A method for fabricating a T-RAM array having a plurality of T-RAM cells, the method comprising the steps of:

providing a semiconductor wafer;

fabricating a thyristor region having a thyristor for each of the plurality of T-RAM cells over the semiconductor wafer; and

fabricating a surrounded gate for each of the plurality of T-RAM cells, wherein the surrounded gate is aligned with a base region of the thyristor;

fabricating a transfer gate region having a transfer gate for each of the plurality of T-RAM cells over at least a portion of the thyristor region.

19. The method according to Claim 18, wherein each of the plurality of T-RAM cells has a size of less than or equal to $8F^2$.

20. The method according to Claim 18, wherein the semiconductor wafer is a semiconductor SOI or bulk wafer.

21. The method according to Claim 18, wherein the thyristor is a vertical thyristor and the transfer gate is a pseudo-TFT transfer gate.

22. The method according to Claim 18, further comprising the step of fabricating first and second wordlines, wherein the first wordline contacts the surrounded gate and the second wordline is integral with the transfer gate.

23. The method according to Claim 18, further comprising the step of fabricating a plurality of bitline contacts throughout the T-RAM array; and

fabricating a plurality of bitlines and a plurality of bitline contacts contacting a respective one of the plurality of bitlines, wherein each of the plurality of bitline contacts connects the respective one of the plurality of bitlines to a junction of the transfer gate.

24. The method according to Claim 18, further comprising the step of providing three layers on the semiconductor wafer prior to the step of fabricating the thyristor region, wherein a first layer is provided on top of a buried oxide layer and is a p-type layer and a second layer is provided on top of the first layer, said second layer is a nitride-oxide layer having a nitride layer below an oxide layer.

25. The method according to Claim 24, wherein the step of fabricating the thyristor region having the thyristor for each of the plurality of T-RAM cells over the semiconductor wafer includes the steps of:

providing a mask over the semiconductor wafer;

etching the oxide layer of the second layer to form etched regions over the nitride layer;

depositing polysilicon within the etched regions;

etching the polysilicon to form a pair of spacer gates for each of the plurality of T-RAM cells;

etching the nitride layer of the second layer to the surface of the first layer to shape the thyristor region; and

growing an n-p-n layer within the thyristor region to form the thyristor.

26. The method according to Claim 25, wherein the step of growing the n-p-n layer includes the steps of:

fabricating a first n-type layer over the first layer using a first n-type doping implant;

fabricating an p-type layer over the first n-type layer using a p-type doping implant; and

fabricating a second n-type layer over the p-type layer by using a second n-type doping implant.

27. The method according to Claim 26, wherein the step of fabricating the first n-type layer includes the step of using n-type doping with a dosage of between $2E13/cm^2$ and $8E14/cm^2$; wherein the step of fabricating the p-type layer includes the step using a p-type doping with a dosage of between $4E13/cm^2$ and $1E14/cm^2$; and wherein the step of fabricating the second n-type layer includes the step of using an n-type doping with a dosage of between $8E14/cm^2$ and $3E15/cm^2$.

28. The method according to Claim 18, wherein the step of fabricating the transfer gate region having the transfer gate for each of the plurality of T-RAM cells over at least a portion of the thyristor region includes the steps of:

fabricating an epi layer over the thyristor region;

providing a dielectric film over the epi layer;

depositing an insulating film over the dielectric film;

forming two gates within the insulating film; and

implanting an n+ dopant within the epi layer to form source and drain regions for the transfer gate.